BNL-Nevis integration test

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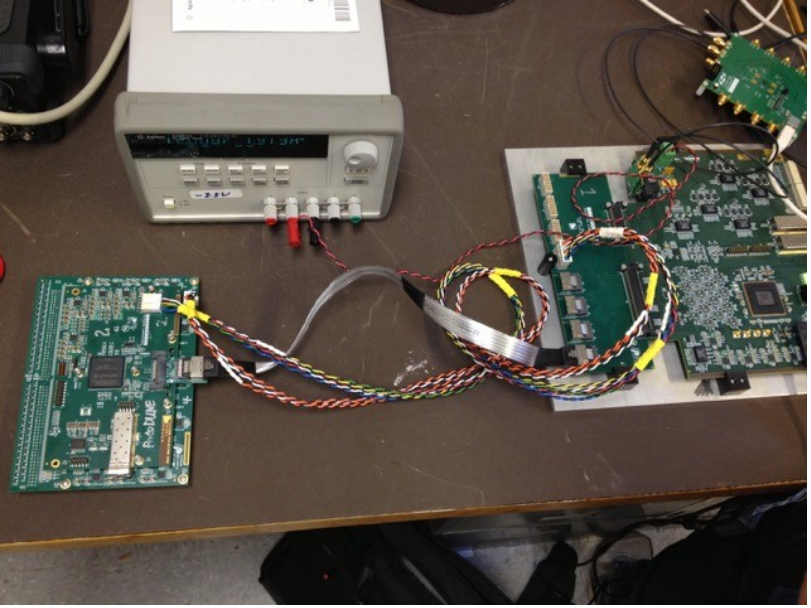
COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

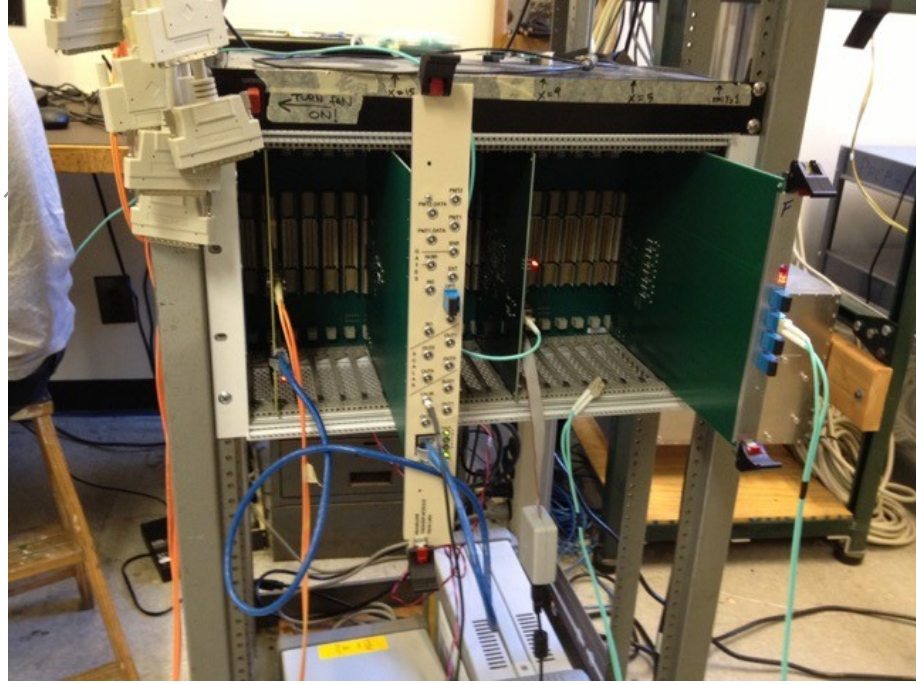
NEVIS LABORATORIES

Goal

- Test optical link between BNL's Warm Interface Board (WIB) and Nevis's Front End Module (FEM).

Setup





ASIC — WIB

Optical

Copper

Magic Blue Box not available.
Used modified uB clock module (16 MHz) directly to WIB (WIB output at 2 MHz)

Clock

Crate

Controller

Trigger

FEM

BNL **Nevis**

Slow readout through controller (no XMIT used)

PCIe card

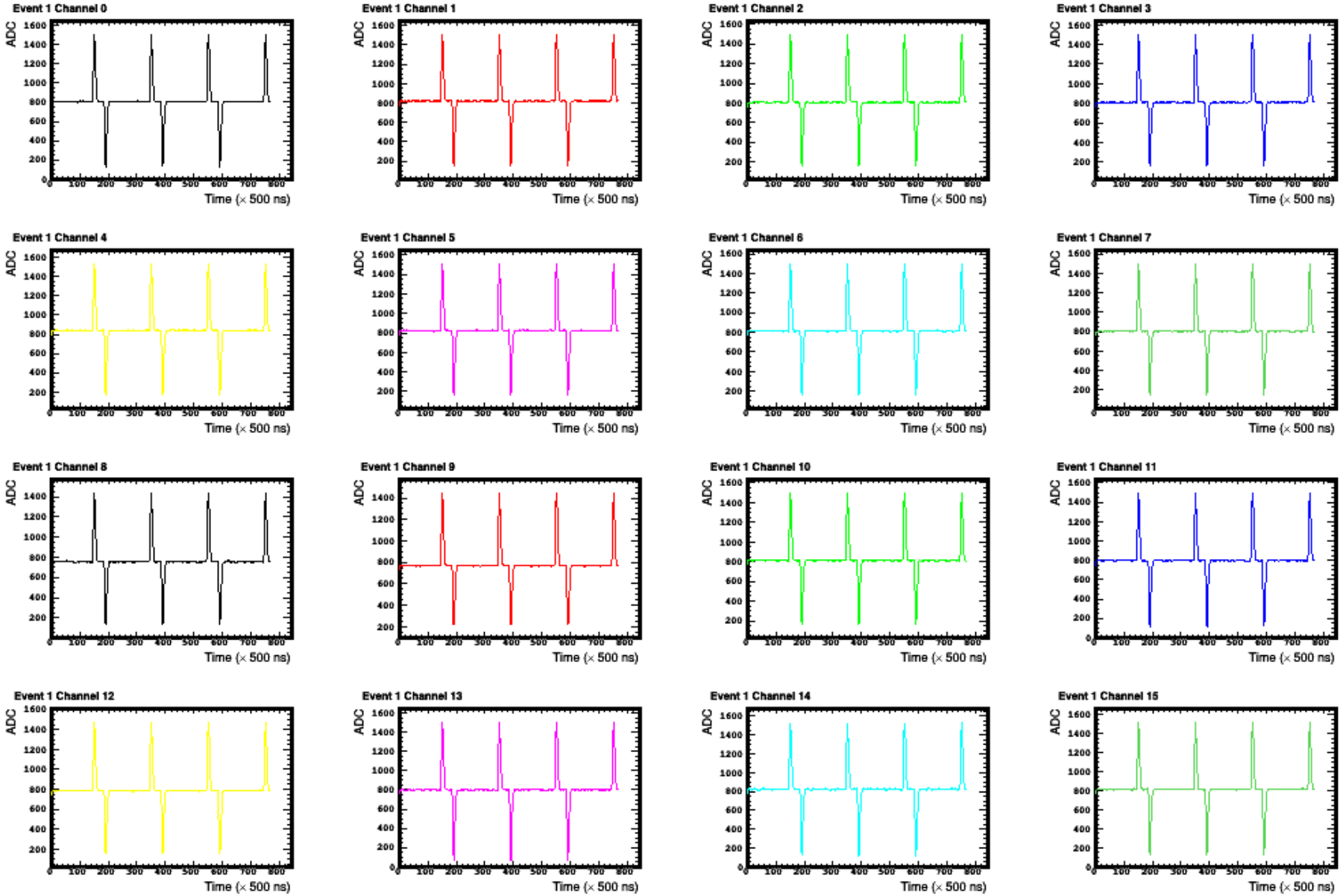
DAQ PC

Trigger sent only to controller:
Asynchronous readout of WIB

Success!

Example

Calibration pulse generated in BNL's ASIC chip 1 (16 channels) read out by Nevis' FEM asynchronously



Lessons learned

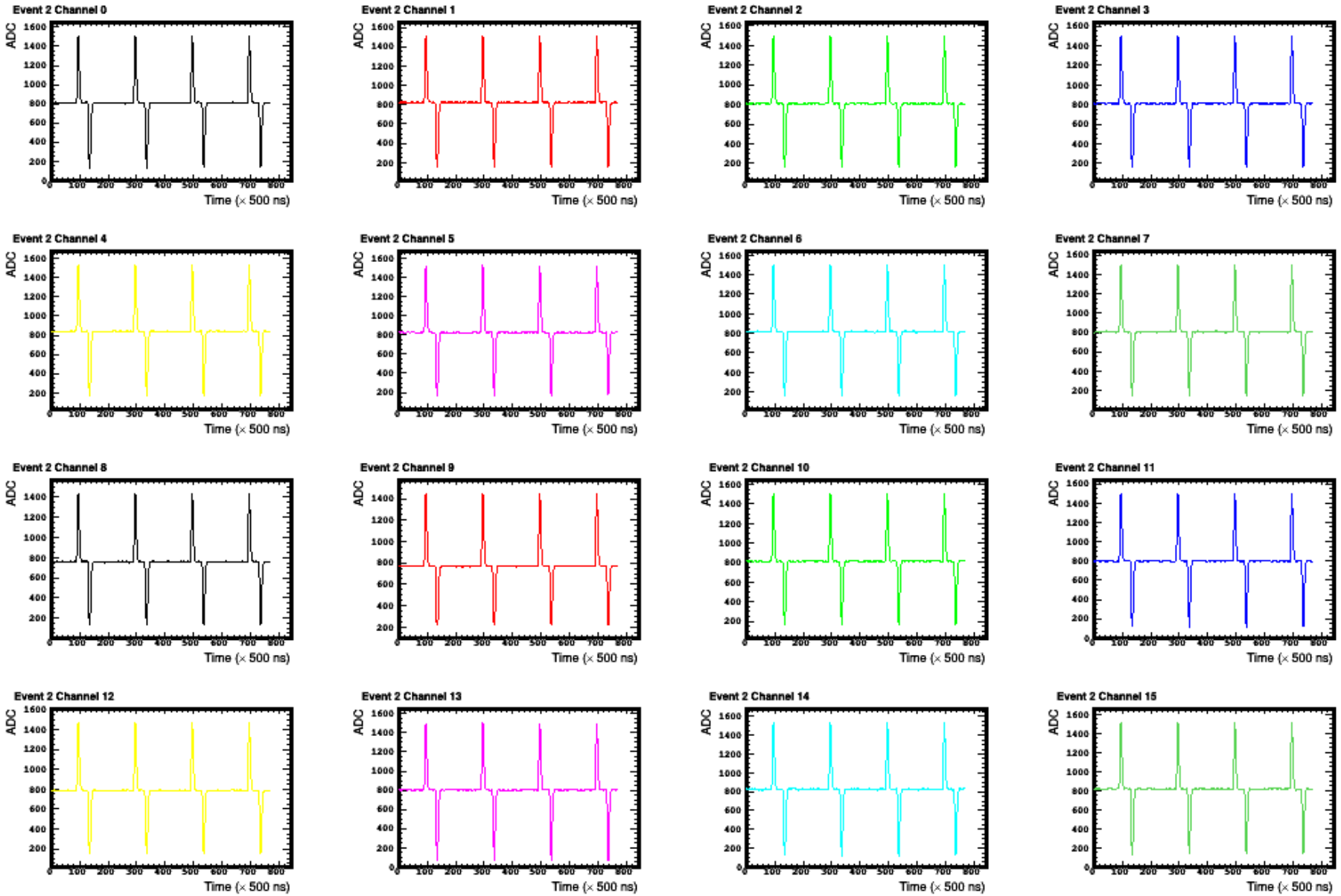
- Successful optical link between BNL's WIB and Nevis' FEM ►Hardware works.
- Need to define a protocol between BNL's WIB and Nevis' FEM for error handling ►Further work needed in FPGAs firmware.

Next test

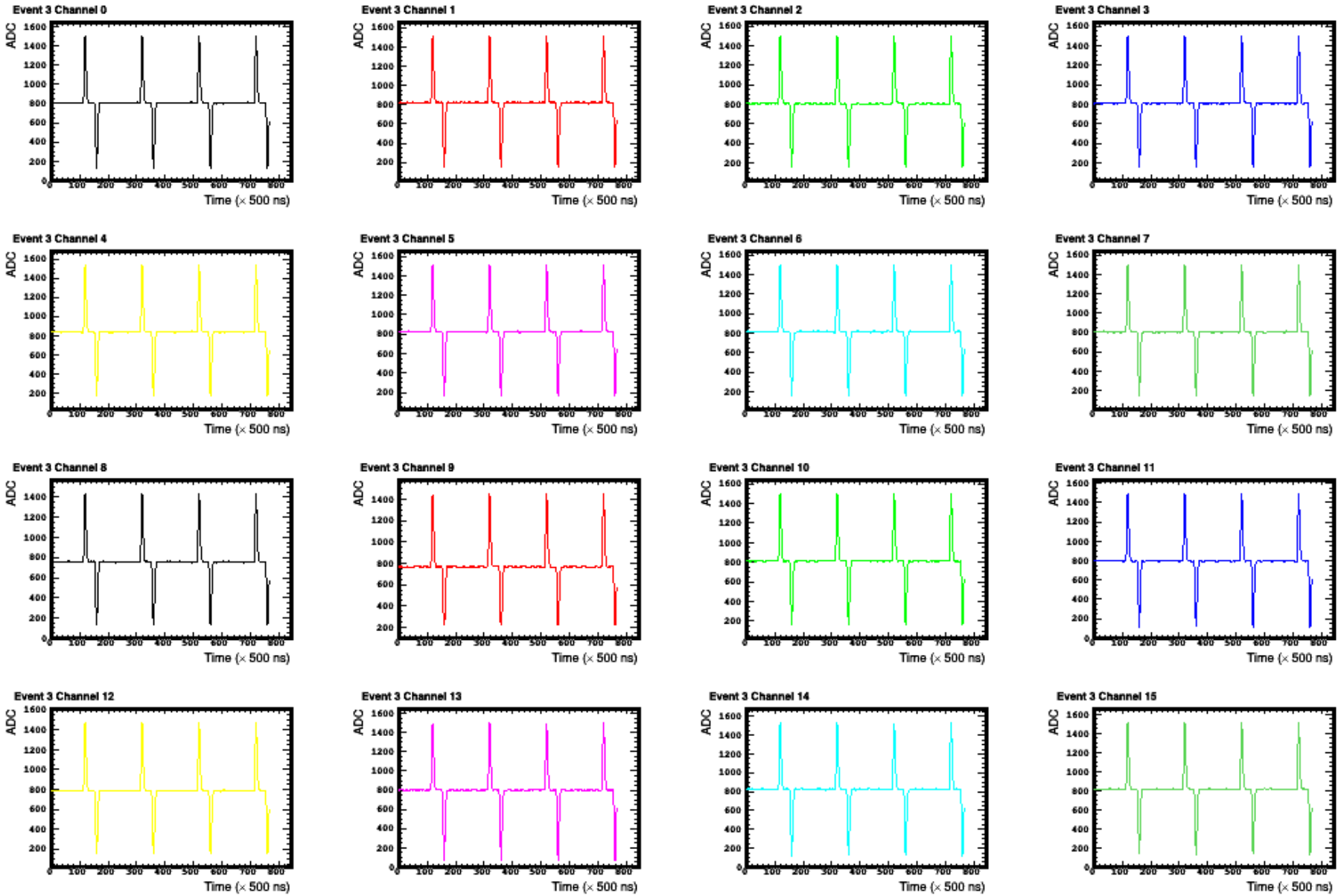
- In November.
- Synchronous readout (BNL receiving calibration pulse from Nevis Trigger Board).
- Using Magic Blue Box? (not critical)
- Longer test ►Control error rate.

Backup

Calibration pulse generated in BNL's ASIC chip 1 (16 channels) read out by Nevis' FEM asynchronously



Calibration pulse generated in BNL's ASIC chip 1 (16 channels) read out by Nevis' FEM asynchronously



Calibration pulse generated in BNL's ASIC chip 1 (16 channels) read out by Nevis' FEM asynchronously